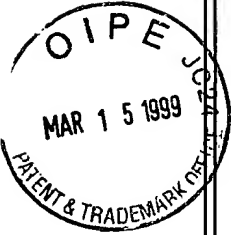


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#32
Appel Brief
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Applicants: Bulucea, Constantin; Rossen, Rebecca
Assignee: Siliconix, Incorporated
Title: TRENCH DMOS POWER TRANSISTOR WITH FIELD-SHAPING
BODY PROFILE AND THREE-DIMENSIONAL GEOMETRY
Serial No.: 08/851,608 Filed: 05/05/97
Examiner: J. Carroll Group Art Unit: 2811
Docket No.: M-799-4C US

San Jose, California

Box AF
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

APPEAL BRIEF UNDER 37 CFR § 1.191

Dear Sir:

Applicants submit this Appeal Brief in triplicate in support of the Notice of Appeal filed in this case on October 19, 1998. An accompanying petition requests a 3-month extension of time, extending the time allowed for filing this appeal brief to March 19, 1999.

The Commissioner is hereby authorized to deduct from Deposit Account No. 19-2386, the amount of \$300.00, being the amount specified in 37 C.F.R. 1.17(c) for this Appeal Brief. The Commissioner is also authorized to deduct any other amounts required for this appeal brief and to credit any amounts overpaid to Deposit Account. No. 19-2386.

I. REAL PARTY IN INTEREST

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300.00 CH The real party in interest is the Assignee, Siliconix, Incorporated.

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SER. NO.08/851,608

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 17-23, 25-42, 44 and 46-65 are pending and rejected.

IV. STATUS OF AMENDMENTS

No amendment was filed since the Final Office Action of May 20, 1998 ("the Final Office Action").

V. SUMMARY OF THE INVENTION

The present invention provides a trench DMOS transistor cell (e.g., cell 21 of Figure 8, discussed in the Specification, from line 11 of page 11 to line 7 of page 12), which includes: (a) a substrate; (b) an epitaxial layer formed on a surface of the substrate with a substantially uniform initial dopant concentration at formation; (c) a body region formed in the epitaxial layer; (d) a source region formed in the epitaxial layer above a portion of the body region; and (e) a trench formed in the epitaxial layer, having substantially vertical side walls, extending from said top surface of the epitaxial layer to a depth d_{tr} . The body region extends, as measured from the top surface of the epitaxial layer, to a first depth d_{max} at a first location and to a lesser depth of d at a second location a predetermined distance from the first location.

Within the trench, the depth d_{tr} is less than the depth d_{max} , and greater than the depth d . The trench of the present invention is (i) closer to the second location than the first location, and (ii) horizontally adjacent the source region; wherein breakdown in the trench DMOS transistor occurs across said epitaxial layer at a position closer to the first location than the second location. In one embodiment, the MOS transistor cell is designed such that depth d_{tr} is less than d_{max} by an amount sufficient to cause semiconductor surface breakdown to occur at a location closer to the first location than the second location (See, for example, Figures 9-15; and in the Specification, from line 17 at page 14 to line 6 of page 16). In another embodiment, the trench DMOS transistor cell includes an epitaxial layer having a thickness d_{epi} small enough to cause semiconductor surface breakdown to occur at a location closer to the first location than the second location. (See, for example, Figure 15; and at the Specification, from lines 14-23 of page 16). In one implementation, the trench, when viewed from above the top surface of the epitaxial structure, is polygonal, having a number of sides greater than four (e.g. six, see Figure 8).

VI. ISSUE

1. Whether or not the Examiner erroneously rejected Claims 17-22, 25-26, 29-30, 32-37, 44, 46-49, 51-58 and 64 under 35 U.S.C. § 103 over U.S. Patent 4,420,379 ("Tonnel"), in view of an article, entitled "A New Vertical Power MOSFET Structure with Extremely Reduced On-resistance" ("Ueda et al."), and further in view of U.S. Patent 4,145,700 ("Jamotkar") and further in view of U.S. Patent 4,376,286 ("Lidow et al. '286").

2. Whether or not the Examiner erroneously rejected Claim 50 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of Lidow et al. '286, further in view of Jambotkar, and further in view of an article, entitled "Optimization of Nonplanar Power MOS Transistors" ("Lisiak et al.").

3. Whether or not the Examiner erroneously rejected Claims 31, 60-62 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of Lidow et al. '286, further in view of Jambotkar, and further in view of an article, entitled "Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation" ("Yamabe et al.").

4. Whether or not the Examiner erroneously rejected Claims 23, 27-28, 38-41, 59-62 and 65 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of the Lidow '286 Patent, further in view of Jambotkar, further in view of Yamabe et al., and further in view of U.S. Patent 4,148,047 ("Hendrickson").

VII. GROUPING OF THE CLAIMS

Claims 17-19, 25 and 29 stand and fall together.

Claims 20, 21, 22 and 26 are each separately patentable.

Claims 23 and 27-28 stand and fall together.

Claim 30 is separately patentable.

Claim 31 is separately patentable.

Claims 32-37 and 44 stand and fall together.

Claims 38-41 stand and fall together.

Claim 42 is separately patentable.

Claims 46-48 and 51 stand and fall together.

Claim 50 is separately patentable.

Claims 52 and 53 stand and fall together.

Claims 54-58 and 64 stand and fall together.

Claims 59 is separately patentable.

Claim 60-62 stand and fall together.

Claim 65 is separately patentable.

VIII. ARGUMENTS

1. Whether or not the Examiner erroneously rejected Claims 17-22, 25-26, 29-30, 32-37, 44, 46-49, 51-58 and 64 under 35 U.S.C. § 103 over Tonnel, in view of Ueda et al., and further in view of Jambotkar, and further in view of Lidow et al. '286.

In the Office Action of October 3, 1997, the Examiner rejected Claims 17-22, 25-26, 29-30, 32-37, 44 and 46 under 35 U.S.C. § 103, stating:

We reject as unpatentable Claims 17 through 22, Claims 25, 26, 29, 30, 32 through 37, 44, 46 through 49, 51 through 58 and 64 under 35 U.S.C. 103 over considerations of Tonnel and Ueda et al., as discussed in the record, but further considered with presently cited and provided Jambotkar and Lidow et al. '286. Jambotkar taught that one may reduce the electric field at a PN-junction between base and drain regions by introducing a close-proximity spacing factor to appropriately space adjacently disposed base regions from one another to accordingly reduce the electric field characteristic thereat and, accordingly, to increase the breakdown voltage characteristic of the device. Lidow et al. similarly taught the appropriate use of the close-proximity spacing factor, as in Jambotkar, but further found advantageous the deeper base regions to accordingly still further

increase the device breakdown voltage characteristic. We thus conclude that one would have accordingly learned therefrom and recognized the improved breakdown voltage characteristic inherently intrinsic of the obvious Tonnel device due to a dramatic reduction of electric field at junction curvature portions thereof. Thus, the present situation comes under the Court's directive that a newly discovered property inherently possessed by things in the prior art does not cause a claim drawn to those things to distinguish over the prior art, after at least *In re Swinehart*, 169 USPQ 226 (CCPA 1971).

In response, in the Amendment of March 24, 1998, Appellants referred the Examiner to Appellants' Preliminary Amendment of May 5, 1997, in which Appellants point out that the combined teachings of Tonnel and Ueda et al. neither disclose nor suggest Applicants Claims 17-22, 24-37, 44 and 46-49:

While Tonnel's Figures 10-12 each show a semiconductor structure having a P-type region 22 being drawn deeper into the substrate 21 than V-slots 31, there is no corresponding verbal teaching in Tonnel's specification regarding this spatial relationship between V-slots 31 and P-type region 22. In other words, the Examiner merely speculates from hindsight that:

Figures 4 through 12, combined with the corresponding written disclosure, plausibly demonstrated deep base regions (22), first introduced in the process step of Figure 4, plausibly grew deeper during the thermal oxidation step of Figure 5, at about the same depth as grooves (30) of Figure 6, and plausibly grew still further deeper than the depth of the grooves during ion implantation and annealing steps subsequently performed in the process steps of Figures 9 and 10.

(emphasis added)

The Examiner's speculation and hindsight reconstruction cannot supplement the absence of teaching in Tonnel regarding the spatial relationship discussed above and recited in Applicants' claims. Further, as amended, Claim 17 recites:

...wherein breakdown in said trench
DMOS transistor occurs across said epitaxial
layer at a position closer to said second location
than said first location.

Thus, Claim 17 recites a limitation regarding the
breakdown characteristics of the trench DMOS transistor
resulting from the aforementioned spatial relationship. Such
breakdown characteristics are neither disclosed nor suggested
by Tonnel, Ueda et al., Lisiak et al., Yamabe et al., or any
combination of their teachings. Similarly, independent Claims
30, 32, 46, 52 and 54 each also recite breakdown characteristics
neither disclosed nor suggested by Tonnel, Ueda et al., Lisiak et
al., Yamabe et al., or any combination of their teachings. Thus,
Applicants believe that the various rejections under 35 U.S.C. §
103 (referenced above) by the Examiner are overcome.

With respect to Jambotkar, which was cited for the first time in the Office Action of
October 3, 1997, Appellants could not find where in Jambotkar the Examiner finds support for
his arguments, since Jambotkar does not teach a "base region". Appellants point out that
Jambotkar, however, teaches "improving the drain-to-substrate reverse breakdown voltage" at
col. 5, lines 22-61:

Also, in the illustrations of FIGS. 10 and 11, only one
outer unbiased annular P region is shown for improving the
drain-to-substrate reverse breakdown voltage through reduction
of electric field at the curvature of the P substrate regions. If
necessary, however, additional one or more outer annular P
regions may be formed, located suitably apart, to reduce the
electric field at the outer periphery of the P regions, and thereby
further improve the drain-to-substrate reverse breakdown
voltage.

... The FET substrate P diffusions are designed to be
located apart from one another by very small distances,
preferably between 4 to 10 micrometers.... The close proximity
of the adjacent substrate diffusions 18 reduces the electric field
in the curvature regions of the inner peripheries of these P
diffusions/N-body junctions, while the presence of unbiased P
diffusions 16 at the appropriate distance from the outer
peripheries of the P substrate diffusions 18 reduces the electric
field in the curvature region of the outer peripheries of those
outer P substrate diffusions 18. As a consequence, the drain to

substrate breakdown voltage is made practically equal to the maximum value which is the plane P to N- junction reverse breakdown value.

Thus, Appellants bring to the Examiner's attention that (a) Jambotkar teaches improving the breakdown voltage exploiting a proximity relationship between annular outer diffusion regions and inner diffusion regions (see Jambotkar's FIGs. 9A, 9B, 10 and 11), and (b) the proximity of annular outer diffusion regions relative to inner diffusion regions has no relevance to Appellants' claims, which recite depths of the body region at various locations relative to a trench.

Similarly, Appellants could not find where in Lidow et al. '286 the Examiner finds support for his arguments. Like Jambotkar, Lidow et al. '286 was cited for the first time in the Office Action of October 3, 1997. Appellants point out that Lidow et al. '286 also do not teach "base regions". Lidow et al. '286, at col. 4, lines 3-12, however, teach a device which "withstand[s] higher reverse voltages":

In a preferred embodiment of the invention, there is an elongated serpentine p(+) conductivity region beneath each of the source electrodes 22 and 23 which thus extends around the serpentine path shown in FIG. 1. These p(+) regions are shown in FIG. 2 as the p(+) regions 30 and 31, respectively, and are similar to those of the prior art except that the maximum p(+) region depth is greatly exaggerated in order to form a large radius of curvature. This allows the device to withstand higher reverse voltages.

Lidow et al. '286 disclose the relative radii of curvature at various locations of the body region. The radii of curvature in Lidow et al. '286 are, however, irrelevant to Applicants' claims, which each recite where breakdown occurs. The locations where breakdown occurs are not specifically taught in Lidow et al. '286. Accordingly, Appellants submit that Applicants' Claims 17-22, 25-26, 29-30, 32-37, 44 and 46 are each patentable

over Tonnel, Ueda et al., Jambotkar and Lidow et al. '286, individually and in any combination.

In response to Appellants' arguments in the Amendment of March 24, 1998, with respect to Jambotkar, the Examiner states in the Final Office Action:

The Applicants indicated on amendment page 3 that Jambotkar did not teach the presence of base regions.

In response, we respectfully disagree because Jambotkar would have disagreed. More particular, Jambotkar advocated a power MOSFET structure that comprised a plurality of closely spaced P-type substrate regions (18) as being analogous to the claimed body region of Claim 17, for example. As disclosed in the sentence beginning on line 63 of column 1, Jambotkar expected that small distances between the body regions produced high voltage capability in the MOSFET. Further, as the Applicants successfully excerpted on amendment page 4, Jambotkar disclosed that the close proximity of adjacently disposed substrate diffusions (18) reduced the electric field in the spherical curvature regions of the inner peripheries of the body diffusions (18).

Appellants are puzzled by the Examiner's analogy between the closely-spaced P-type substrate regions 18 of Jambotkar and Appellants' body region of Claim 17. While Jambotkar shows closely-paced diffusion regions 18 in its Figures 2A-9A, and teach that such closely-spaced diffusion regions reduce the electric fields in the inner peripheries, no such closely-spaced structure is recited in Claim 17. Claim 17 recite a single body region, not multiple closely-spaced diffusion regions:

a body region of a second conductivity type formed in said epitaxial layer, said body region extending, as measured from said top surface of said epitaxial layer, to a first depth d_{\max} at a first location and to a depth of d at a second location, where d is less than d_{\max} , said first and second locations being separated by a predetermined horizontal distance;

Thus, Appellants' respectfully submit that the Examiner has not shown how "one would have accordingly learned therefrom and recognized the improved breakdown voltage characteristic inherently intrinsic of the obvious Tonnel device due to a dramatic reduction of electric field at junction curvature portions thereof," and further how that learning can be combined with the teachings of Tonnel, Ueda et al., and Lidow et al. '286 to be relevant to Appellants' claims.

Similarly, with respect to Lidow et al. '286, the Examiner states in the Final Office Action:

The Applicants indicated on amendment page 5 that large radii of curvature of deep body regions that helpfully assist a power MOSFET to withstand high reverse voltages, as taught by Lidow et al. in the paragraph beginning on line 36 of column 6 and, further, as successfully excerpted by the Applicants on amendment page 4, stand as irrelevant to the presently claimed subject matter because Lidow et al. allegedly never taught where the breakdown occurred.

In response, we respectfully disagree because Lidow et al. would have disagreed. One firstly would have recognized that radii of curvature, as discussed by Lidow et al., had every thing to do with diffusion depth, evidently from the presently cited excerpt from the Sze monograph, provided as a reference of interest. Secondly, one would have recognized that electric fields at the deep curvature body junctions far exceeded electric fields at flat, planar body junctions. We thus conclude that Lidow et al. expressed where likely breakdown would have occurred. As such, the Lidow et al. teachings are completely analogous to the presently claimed structure.

Again, Appellants are puzzled by the Examiner's reasoning. In the Sze monograph, diffusion contours of constant doping concentration are obtained using a 2-dimensional diffusion equation. Sze shows concentrations of dopants diffusing from the surface downward into the substrate and laterally into a region protected by a diffusion mask. Sze

indicates as "radii of curvature" the distances into the substrate corresponding to various dopant concentration to surface concentration ratios. How the teachings of Sze applies to Claim 17 in the instant case, the Examiner does not explain. In addition, the Examiner's statement "one would have recognized that electric fields at the deep curvature body junctions far exceeded electric fields at flat, planar body junctions" appears totally unsupported. The Examiner did not show from which reference he derives this teaching. Even if the Examiner is correct, the Examiner did not relate this teaching to those of Lidow et al. '286. The Examiner still has not show how Lidow et al. '286 suggest that the breakdown "occurs across said epitaxial layer at a position closer to said first location than said second location", as recited in Appellants' Claim 17. In summary, the Examiner fails to show how Lidow et al. '286 can be combined with the teachings of Tonnel, Ueda et al., and Jambotkar to be relevant to Appellants' Claim 17. Appellants would like to point out again that Lidow et al. '286 teach that a higher reverse voltage can be achieved, but does not teach the location of where breakdown occurs.

Accordingly, Appellants respectfully submit that Claims 17 and its dependent Claims 18-22, 25-26 and 29 are patentable over the combined teachings of Tonnel, Ueda et al., Jambotkar and Lidow et al. '286. Claim 30 recites limitations relating to the relative depths of the third covering layer and the trench, similar to those discussed above with respect to Claim 17. Thus, Claim 30 is similarly patentable over the combined teachings of Tonnel, Ueda et al., Jambotkar and Lidow et al. '286. Claim 32 recites limitations relating to the relative depths of the body region and the trench, similar to those discussed above with respect to Claim 17. Thus, Claim 30 and its dependent Claims 33-37, 44 are similarly each patentable over the combined teachings of Tonnel, Ueda et al., Jambotkar and Lidow et al. '286. Claim

46 recites limitations relating to the relative depths of a portion P of a second region and the trench, similar to those discussed above with respect to Claim 17. Thus, Claim 46 and dependent Claims 47-49 and 51 are similarly each patentable over the combined teachings of Tonnel, Ueda et al., Jambotkar and Lidow et al. '286. Claim 52 recites limitations relating to the relative depths of the deepest part of a third region and the trench similar to those discussed above with respect to Claim 17. Thus, Claim 52 and dependent Claim 53 are similarly patentable over the combined teachings of Tonnel, Ueda et al., Jambotkar and Lidow et al. '286. Claim 54 recites limitations relating to the relative depths of the body region and the trench similar to those discussed above with respect to Claim 17. Thus, Claim 54 and dependent Claims 55-58 and 64 are similarly each patentable over the combined teachings of Tonnel, Ueda et al., Jambotkar and Lidow et al. '286.

Since Claims 20-22, 26 and 49 each recite limitations, enumerated in the following paragraphs, that are neither disclosed nor suggested by the combined teachings of Tonnel, Ueda et al., Jambotkar and Lidow et al. '286, these claims are further each separately patentable over these references:

- a. Claim 20 recites that "depth d_{tr} is less than d_{max} by an amount sufficient to cause semiconductor surface breakdown to occur at a location closer to said first location than said second location".
- b. Claim 21 recites that "said epitaxial layer has a thickness d_{epi} small enough to cause semiconductor surface breakdown to occur at a location closer to said first location than said second location".
- c. Claim 22 recites that "when viewed from above said top surface of said epitaxial structure, is polygonal, having a number of sides greater than four."

d. Claim 26 recites that "said gate oxide [has] a thickness sufficient to cause semiconductor breakdown to occur at a location closer to said first location than said second location."

e. Claim 49 recites that "said avalanche breakdown is a reach-through breakdown across said second portion."

Therefore, for the above reasons, Appellants believe that the Examiner's rejection of Claims 17-22, 25-26, 29-30, 32-37, 44, 46-49, 51-58 and 64 is erroneous and should be reversed.

2. Whether or not the Examiner erroneously rejected Claim 50 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of the Lidow et al. '286, further in view of Jambotkar, and further in view of Lisiak et al.

In the Office Action of October 3, 1997, the Examiner rejected Claim 50 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of Lidow et al. '286, further in view of Jambotkar, and further in view of Lisiak et al., stating:

We reject Claim 50 as unpatentable under 35 U.S.C. 103 over considerations of Tonnel, Ueda *et al.*, Lidow *et al.* '286, Jambotkar and Lisiak *et al.*, as discussed *supra* and in the record.

In response, in the Amendment of March 24, 1998, Appellants referred the Examiner to Appellants' Preliminary Amendment of May 5, 1997, which shows that the teachings of Tonnel, Ueda et al., and Lisiak et al. neither disclose nor suggest Claim 50 (Claim 50 depends from Claim 46). Appellants further point out, as discussed in the previous section above, that the teachings of Jambotkar and Lidow et al. '286 are irrelevant to Claim 50, which recites

where a breakdown occurs. Thus, Appellants have shown in the Amendment of March 24, 1998 that the Examiner's rejection of Claim 50 is erroneous.

Since the Examiner did not specifically comment in the Final Office Action on Appellants' arguments in the Amendment of March 24, 1998, Appellants respectfully request that the Examiner's rejection of Claim 50 be reversed based on the arguments of record.

3. Whether or not the Examiner erroneously rejected Claims 31, 60-62 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of Lidow et al. '286, further in view of Jambotkar, and further in view of Yamabe et al.

In the Office Action of October 3, 1997, the Examiner rejected Claims 31 and 60-62 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of Lidow et al. '286, further in view of Jambotkar, and further in view of Yamabe et al. The Examiner states:

We reject Claims 31, 60, 61 and 62 under 35 U.S.C. 103 over considerations of Tonnel, Ueda et al., Jambotkar, Lidow et al. '286 and Yamabe et al., as discussed supra and in the record.

Noting that the Examiner did not previously apply Yamabe et al. to Claim 31 in previous office actions, Applicants responded to the Examiner in the Amendment of March 24, 1998, assuming that it was Claim 41 that the Examiner intended in this rejection. Based on that assumption, Appellants referred the Examiner to Appellants' Preliminary Amendment of May 5, 1997, which points out that Tonnel, Ueda et al., and Yamabe et al. neither disclose nor suggest Applicants' Claims 41 and 60-62. Appellants further point out that the teachings of Jambotkar and Lidow et al. '286 are irrelevant to Claims 41 and 60-62, which each recite where a breakdown occurs.

In response to Appellants' arguments in the Amendment of March 24, 1998, the Examiner states in the Final Office Action:

The Applicants incorrectly assumed, on amendment page 6, that an excerpt on the last three lines of amendment page 5 erroneously cited Claim 31.

Responding now to the Examiner's rejection of Claim 31, Claim 31 recites:

31. A trench DMOS transistor cell as in Claim 30, wherein said trench comprises rounded edges of oxidized material.

Since Claim 31 depends from Claim 30, Claim 31 is at least patentable over Tonnel, Ueda et al., Lidow et al. '286, Jambotkar and Yamabe et al., for the reasons stated above with respect to Claim 30 above under the discussion of Issue (1), Yamabe et al. providing no teaching with respect to where breakdown occurs. Likewise, Claim 60-62, each depending from Claim 54, are patentable over Tonnel, Ueda et al., Lidow et al. '286, Jambotkar and Yamabe et al., at least for the reasons stated above with respect to Claim 54 above under the discussion of Issue (1). Accordingly, Appellants respectfully submit that the Examiner's rejection of Claims 31, 60-62 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of Lidow et al. '286, further in view of Jambotkar, and further in view of Yamabe et al is erroneous and respectfully request that the rejection be reversed.

4. Whether or not the Examiner erroneously rejected Claims 23, 27-28, 38-41, 59-62 and 65 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of Lidow et al. '286, further in view of Jambotkar, further in view of Yamabe et al., and further in view of Hendrickson.

In the Office Action of October 3, 1997, the Examiner rejected Claims 23, 27-28, 38-41, 59-62 and 65 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of Lidow et al. '286, further in view of Jambotkar, further in view of Yamabe et al., and further in view of Hendrickson, stating:

We reject Claims 23, 27, 28, 38, 39, 40, 41, 59, 60, 61, 62 and 65 under 35 U.S.C. 103 Tonnel, Ueda *et al.*, Jambotkar, Lidow *et al.* '286 and Yamabe *et al.*, as discussed *supra*, but further considered with presently cited and provided Hendrickson who suggested, with Figure 14, that a device similar to the obvious Tonnel device, may be advantageously replicated into the hexagonal pattern across the wafer surface. We thus conclude it to have been obvious for one to have accordingly replicated the obvious Tonnel device.

Since Claims 23, 27-28, 38-41, 59-62 and 65 each depend from one of Claims 17, 32 and 54, Appellants respectfully submit that Claims 23, 27-28, 38-41, 59-62 and 65 are at least patentable for the reasons discussed above under Issue (1) with respect to Claims 17, 32 and 54.

Noting that the Examiner did not previously apply Yamabe et al. to Claims 23, 27-28 and 38, Appellants point out in the Amendment of March 24, 1998 to the Examiner that, in the previous office actions, the Examiner relied upon Yamabe et al. for the teachings:

Yamabe et al. taught at least the leakage current advantage of performing etching to remove a sacrificial oxide layer to round corners of trenches accommodating insulated gate electrodes, like those anticipated by Ueda et al. and envisaged by Tonnel. We thus conclude it to have been obvious for one to have performed rounding of trenches accommodated insulated gate electrodes to gain the leakage current advantage in trench insulated gate transistors like those envisaged by Tonnel.

(Paper 3, Office Action of April 4, 1996)

Appellants responded in the Amendment of March 24, 1998 to the Examiner's rejection based on the above-quoted teaching of Yamabe et al.. Since Claims 23, 27-28, 38, 59 and 65 each recite a cell configuration, Appellants thus point out to the Examiner that the above-quoted teaching of Yamabe et al. on which the Examiner previously relied appears to have no relevance to these claims. Since Appellants have previously shown in the Preliminary Amendment of May 5, 1997 that Claims 27-28 and 65 are patentable over Tonnel in view of Ueda et al., and since the Examiner did not previously reject Claims 38 and 59 under 35 U.S.C. § 103, Appellants thus believe that Claims 27-28, 38, 59 and 65 are patentable over Tonnel, in view of Ueda et al. and Yamabe et al.

With respect to Claims 39, 40-41, and 60-62, Appellants also point out that Appellants' Preliminary Amendment of May 5, 1997 shows that these claims are patentable over Tonnel, in view of Ueda et al., and Yamabe et al.

In response to Appellants' arguments in the Amendment of March 24, 1998, the Examiner states in the Final Office Action:

The Applicants incorrectly alleged on amendment page 7 that the teachings of Yamabe et al. have no relevance to at least Claim 23. At least Claim 23, however, called for a trench. The Yamabe et al. teachings are relevant at least to a trench. We thus conclude that the Applicants have inadequately appreciated that the applied prior art documentation rendered obvious the presently claimed subject matter.

Appellants do not argue with the Examiner that the teachings of Yamabe et al. are relevant to a trench. In the Amendment of March 24, 1998, Appellants were simply asking the question as to whether the Examiner deems Yamabe et al. to be teaching that the "number of sides [of the trench viewed from above] is six." From the Examiner's response in the Final

Office Action, it appears that the Examiner does not deem Yamabe et al. to be teaching this limitation.

In the Amendment of March 24, 1998, Appellants point out that, contrary to the Examiner's assertion, Hendrickson does not teach extending the Tonnel device to a hexagonal surface over a wafer surface. Since Appellants read Hendrickson to be teaching merely triangular and rectangular cells (see Hendrickson's FIGs. 2, 3A, 3B, 6, 10), Appellants respectfully requested the Examiner to indicate with particularity where he finds support in Hendrickson regarding the "hexagonal pattern." In response to this request, the Examiner states in the Final Office Action:

In response, Hendrickson, on line 60 of column 5, referred to the pattern shown in Figure 3A as possessing "six-fold symmetry;" Hendrickson, on line 22-23 of column 6, referred to six-fold symmetry patterns as desirably forming densely packed "hexagonal" matrix structures. Considering that Hendrickson expected one to have advantageously applied hexagonal matrix structures to V-groove MOSFET embodiment disclosed in Figure 14, much like that disclosed by Tonnel, we conclude it to have been obvious for one to have accordingly disposed the obvious U-slot alternative suggested by Tonnel, into the advantageous hexagonal pattern advocated by Hendrickson. We thus conclude that the Applicants have inadequately considered the record, their presently claimed subject matter, and the demonstration in the record that the applied prior art documentation rendered obvious the presently claimed subject matter.

Appellants respectfully submit that the Examiner is in error. As shown in Hendrickson's Figures 3A-3C, while Hendrickson teaches a densely packed hexagonal matrix structure, Hendrickson achieves this hexagonal matrix structure using cells with triangular diffusion areas, as viewed from the top surface (Figures 3A-3C). In fact, Hendrickson does not teach that its cell structures are hexagonal. For example, in FIGs. 3A and 3C,

Hendrickson shows two types of quadrilateral "unit cells". Thus, Appellants respectfully submit that Hendrickson neither discloses or suggests Claim 23's hexagonal trench.

For these reasons, Appellants respectfully submit that the Examiner's rejection of Claims 23, 27-28, 38-41, 59-62 and 65 under 35 U.S.C. § 103 over Tonnel in view of Ueda et al., further in view of Lidow et al. '286, further in view of Jambotkar, further in view of Yamabe et al., and further in view of Hendrickson is erroneous and respectfully request that the rejection be reversed.

IX. CONCLUSION

For the above reasons, Appellants respectfully submit that the Examiner's various rejections of pending Claims 17-23, 25-42, 44 and 46-65 are unfounded. Accordingly, Appellants request that the rejections of claims 17-23, 25-42, 44 and 46-65 be reversed.

Claims 42 and 63 are not specifically rejected in any of the Examiner's rejections except under the judicial doctrine of obviousness type double-patenting. Accordingly, Appellants will submit a terminal disclaimer upon Claims 42 and 63, and all other claims the Examiner indicates as allowable over the prior art of record.

APPENDIX

The pending claims are set forth as follows:

17. A trench DMOS transistor cell, comprising:

a substrate of a first conductivity type, said substrate having a surface;

an epitaxial layer of said first conductivity type formed on said surface of said substrate, said epitaxial layer having a top surface and a bottom surface, said epitaxial layer having a substantially uniform initial dopant concentration at formation;

a body region of a second conductivity type formed in said epitaxial layer, said body region extending, as measured from said top surface of said epitaxial layer, to a first depth d_{\max} at a first location and to a depth of d at a second location, where d is less than d_{\max} , said first and second locations being separated by a predetermined horizontal distance;

a source region of said first conductivity type formed in said epitaxial layer above a portion of said body region, said portion of said body region being located between said second location and said source region; and

a trench formed in said epitaxial layer, having substantially vertical side walls, extending from said top surface of said epitaxial layer to a depth d_{tr} , said depth d_{tr} being less than said depth d_{\max} , and greater than said depth d , said trench being (i) closer to said second location than said first location, and (ii) horizontally adjacent said source region; wherein breakdown in said trench DMOS transistor occurs across said epitaxial layer at a position closer to said first location than said second location.

18. A trench DMOS transistor cell as in Claim 17, wherein said body region has a portion exposed at said top surface of said epitaxial layer.

19. A trench DMOS transistor cell as in Claim 18, wherein said source region has a portion exposed at said top surface of said epitaxial layer.

20. A trench DMOS transistor cell as in Claim 17, wherein depth d_{tr} is less than d_{max} by an amount sufficient to cause semiconductor surface breakdown to occur at a location closer to said first location than said second location.

21. A trench DMOS transistor cell as in Claim 17, wherein said epitaxial layer has a thickness d_{epi} small enough to cause semiconductor surface breakdown to occur at a location closer to said first location than said second location.

22. A trench DMOS transistor cell as in Claim 17, wherein said trench, when viewed from above said top surface of said epitaxial structure, is polygonal, having a number of sides greater than four.

23. A trench DMOS transistor cell as in Claim 22, wherein said number of sides is six.

25. A trench DMOS transistor cell as in Claim 17, wherein said trench comprises polysilicon isolated from said source and body regions by a layer of gate oxide.

26. A trench DMOS transistor cell as in Claim 21, wherein said gate oxide having a thickness sufficient to cause semiconductor breakdown to occur at a location closer to said first location than said second location.

27. A semiconductor wafer comprising a predetermined number of trench DMOS transistor cells in an closed cell configuration, each trench DMOS transistor cell in said semiconductor wafer being a DMOS trench transistor cell as recited in Claim 17.

28. A semiconductor wafer comprising a predetermined number of trench DMOS transistor cells in an open cell configuration, each trench DMOS transistor cell in said semiconductor wafer being a DMOS trench transistor cell as recited in Claim 17.

29. A trench DMOS transistor cell as in Claim 17, wherein said substrate has a dopant concentration higher than said initial dopant concentration of said epitaxial layer, said substrate and said epitaxial layer forming respectively drain and drift regions of said trench DMOS transistor cell.

30. A trench DMOS transistor cell, comprising:

a substrate of semiconductor material of a first electrical conductivity type having a top surface;

a first covering layer of semiconductor material of said first electrical conductivity type, said first covering layer (i) having a dopant concentration less than that of said substrate, (ii) having a top surface and (iii) being contiguous to and overlying the substrate top surface;

a second covering layer of semiconductor material of second electrical conductivity type having a top surface and being contiguous to the top surface of the

first covering layer and extending vertically downward from the top surface of the first covering layer into an upper portion of the first covering layer;

a third covering layer of semiconductor material of said first electrical conductivity type having a top surface and being contiguous to and partly overlying the top surface of the second covering layer, where the maximum depth of the second covering layer relative to the top surface of the third covering layer is a depth d_1 ;

a trench, having side walls and a bottom wall, said side walls extending vertically downward from the top surface of the third covering layer through the third and second covering layers and through a portion of, but not all of, the first covering layer, where the trench has a maximum depth relative to the top surface of the third covering layer equal to a second depth d_2 and d_2 is less than d_1 ;

a layer of oxide positioned within the trench and contiguous to the bottom walls and side walls of the trench so that portions of the trench are filled with the oxide layer;

electrically conducting semiconductor material, contiguous to the oxide layer and positioned within the trench so that the oxide layer lies between the electrically conducting semiconductor material and the bottom and side walls of the trench; and

three electrodes that are electrically coupled to the electrically conducting semiconductor material in the trench, to the third covering layer and to the substrate, respectively; wherein junction breakdown occurs away from the trench and into a portion of the second covering layer.

31. A trench DMOS transistor cell as in Claim 30, wherein said trench comprises rounded edges of oxidized material.

32. A trench DMOS transistor cell, comprising:

a substrate;

an epitaxial layer above the substrate;

a trench in the epitaxial layer, the trench having substantially vertical side walls and having a predetermined depth d_{tr} ; and

a body region in the epitaxial layer, the body region having a predetermined maximum depth d_{max} ; wherein the depth d_{tr} is less than the depth d_{max} , and wherein junction breakdown occurs away from the trench and into the epitaxial layer.

33. A trench DMOS transistor cell as in Claim 32, wherein the substrate is of a first conductivity type, the epitaxial layer is of said first conductivity type and the body region is of a second conductivity type.

34. A trench DMOS transistor cell as in claim 33 wherein the epitaxial layer has a top surface and the body region extends from the epitaxial layer top surface into an upper portion of the epitaxial layer.

35. A trench DMOS transistor cell as in claim 34 wherein a source region is formed in said epitaxial layer.

36. A trench DMOS transistor cell as in Claim 34 wherein an epitaxial region partially covers the body region.

37. A trench DMOS transistor cell as in Claim 36 wherein the body region includes a heavily doped body region extending upward through the epitaxial region and forming an exposed pattern at the epitaxial layer top surface.

38. A trench DMOS transistor cell as in Claim 37 wherein the trench surrounds the exposed pattern of the heavily doped body region.

39. A trench DMOS transistor cell of Claim 32 wherein the trench has side walls, said DMOS transistor cell having an oxide layer on said trench walls; and wherein said oxide layer is etched to create rounded corners in said trench.

40. A trench DMOS transistor cell as in Claim 39, further comprising a gate oxide layer within the trench.

41. A trench DMOS transistor cell of Claim 40 further comprising electrically conducting material contiguous to the gate oxide layer, wherein the gate oxide layer is located between the electrically conducting material and the trench.

42. A trench DMOS transistor as in Claim 40, further comprising:
a first polysilicon layer on a portion of said gate oxide layer;

a second oxide layer on a portion of said first polysilicon layer;
a second polysilicon layer on a portion of said second oxide layer; and
a metal layer wherein said first polysilicon layer extends from the trench to a field region creating an electrical contact to the metal layer and providing continuity from the metal layer to the trench.

44. A trench DMOS transistor cell as in Claim 32 wherein a horizontal cross section of the cell has a polygonal shape.

46. A transistor, comprising:

a first region of a first conductivity type;
a second region of a second conductivity type over said first region;
a third region of said first conductivity type such that said first and third regions are separated by said second region;
a trench, having substantially vertical side walls, extending through said third and second regions; and
a gate in said trench; wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.

47. A transistor as in claim 46 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.

48. A transistor as in Claim 46 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.

49. A transistor as in Claim 48 wherein said avalanche breakdown is a reach-through breakdown across said second portion.

50. A transistor as in Claim 46 wherein said portion P of said second region extends deeper than said trench by more than 0.5 μm .

51. A transistor as in Claim 46 further comprising an insulator between said surface of said trench and said gate.

52. A transistor, comprising:

a first region of a first conductivity type;

a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;

a third region of a second conductivity type over said second region, said second and third regions forming a junction;

a fourth region of said first conductivity type over said third region;

a trench, having substantially vertical side walls, extending through said fourth and third regions; and

a gate in said trench; wherein a deepest part of said third region is laterally spaced from said trench; and wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.

53. A transistor as in claim 52 wherein the deepest of said third region is doped heavier than a part of said third region which part is adjacent said trench.

54. A semiconductor device comprising:

a semiconductor structure having a trench therein of depth d_{tr} and substantially vertical side walls, said semiconductor structure including a drain region, a source region, a body region, and a gate region within said trench and separated from said body region by a dielectric material, said body region having a maximum depth of d_{max} , wherein said maximum depth d_{max} being greater than said depth d_{tr} and wherein junction breakdown occurs away from said trench.

55. A semiconductor device as in Claim 54, further comprising a substrate of a first conductivity type, an epitaxial layer of said first conductivity type and wherein said body region is of a second conductivity type.

56. A semiconductor device as in claim 55 wherein the epitaxial layer has a top surface and the body region extends from a surface of the epitaxial layer into an upper portion of the epitaxial layer.

57. A semiconductor device as in claim 55 wherein a source region is formed in said epitaxial layer.

58. A semiconductor device as in Claim 55 wherein said body region extends upward through the epitaxial layer and forming an exposed pattern at a surface of said epitaxial layer.

59. A semiconductor device as in Claim 58 wherein the trench surrounds the exposed pattern of the body region.

60. A semiconductor device as in Claim 54 wherein said trench has side walls, said semiconductor device having an oxide layer on said trench walls, and wherein said oxide layer is etched to create rounded corners in said trench.

61. A semiconductor device as in Claim 60, further comprising a gate oxide layer within the trench.

62. A semiconductor device as in Claim 61 further comprising an electrically conducting material contiguous to said gate oxide layer, wherein said gate oxide layer is located between said electrically conducting material and said trench.

63. A semiconductor device as in Claim 61, further comprising:
a first polysilicon layer on a portion of said gate oxide layer;
a second oxide layer on a portion of said first polysilicon layer;
a second polysilicon layer on a portion of said second oxide layer; and
a metal layer wherein said first polysilicon layer extends from the trench to a field region creating an electrical contact to the metal layer and providing continuity from the metal layer to the trench.

64. A semiconductor device as in Claim 54, further comprising an electrical contact to the gate region, the drain region and simultaneously to the body region and the source region.

65. A semiconductor device as in Claim 54 wherein a horizontal cross section of said semiconductor body has a polygonal shape.

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3/8/99

Date of Signature

Respectfully submitted,



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